EE/CprE/SE 491 WEEKLY REPORT 1

Date: ***January 24th, 2023 – February 5th***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Weekly Summary

This first week was mainly getting the expectations of the project and an introduction to the Efabless tools. As a team, we were able to set up a weekly meeting with both our advisor and client. The majority of the other work we did was researching the tools that were relevant to the Efabless open MPW shuttle. As a group, we identified the major open-source software tools that will be needed for the analog design process flow. We also located GitHub repositories that contained sample user projects that were created on the Caravel Harness. Work has begun on cloning these repositories and simulating them.

Past week accomplishments

- Joshua Thater
    - Researched the open-source software that is used during the analog design process. The main tools are XSCHEM which is used for schematic drawing, NGSPICE, which is used for simulation testing, MAGIC which is used for making layouts & NETGEN, which will run LVS tests on the layout.
    - Got reacquainted with the basics of GitHub.
    - Created a Virtual Machine and began downloading all of the open-source software.
    - Looked over past ReRAM projects that had been approved for the open MPW.

    - Attempted to clone the GitHub repo of the Caravel Harness.
- Aiden Petersen
    - Made progress in setting up the caravel framework.
        - Setup git repository
        - Attempted to create a docker container for easy deployment
    - Extensively read caravel documentation and forums to get the framework setup.
    - Set up Linux virtual machine to run necessary tools on.
- Matt Ottersen
    - Got acquainted with tools that will be used throughout the design process using the Open Galaxy VM
- Regassa Dukele
    - Download and set up some software used to design analog and start proper documentation of essential tools(software) necessary for design like XSCHEM and NGSPICE.

Pending issues

- Cloning the Caravel Harness repository and running the simulation.
- Obtaining past ReRAM projects and uploading their schematics into XSCHEM.
- Learning more about the Efabless tape-out process

Individual contributions

Team Member	Individual Contributions	Weekly Hours	Total Hours
Joshua Thater	Researched the analog design process that Efabless uses. Began downloading open-source software that will be used to design and test analog components.	8	8
Aiden Petersen	Setting up Caravel framework	6	6
Matt Ottersen	Used design tools	5	5
Regassa Dukele	Downloaded software	5.5	5.5

Plans for the upcoming week

- Joshua Thater
    - Finish downloading all of the open-source software.
    - Upload past ReRAM project into XSCHEM & look into how it was made.
- Aiden Petersen
    - Determine if we need to use the digital or analog caravel framework (our project is mixed-signal)
    - Finish setting up the caravel framework

    - Harden and simulate an example design.
- Matt Ottersen
    - Download and set up all of the open source software
    - Look into ReRAM designs
- Regassa Dukele
    - Download and set up some software